Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (currently amended): A method comprising:

receiving an input clock signal representing either a differential clock signal or a single-ended clock signal;

determining whether the input clock signal is a differential clock signal or a single-ended clock signal; ~~and~~

automatically generating an output clock signal based on the determination; and

compensating for delay between the input clock signal and the output clock signal.

2. (original): The method of claim 1 wherein generating the output clock signal comprises generating a single-ended output clock signal when the input clock signal is determined to be a differential clock signal.

3. (original): The method of claim 1 wherein the generated clock signal has the same frequency as the input clock signal.

4. (currently amended): A method comprising:

receiving an input clock signal representing either a differential clock signal or a single-ended clock signal;

determining whether the input clock signal is a differential clock signal or a single-ended clock signal; ~~and~~

automatically generating an output clock signal based on the determining;

wherein receiving the input clock signal comprises receiving a single-ended clock signal on a first input terminal and a ground potential on a second input terminal; and

aligning the input clock signal and the output clock signal, wherein the aligning the input clock signal and the output clock signal comprises compensating for delay of the output clock signal.

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5. (original): The method of claim 1 further comprising generating a clock mode signal based on the determination.

6. (cancelled)

7. (original): The method of claim 5 wherein the output clock signal is a single-ended clock signal generated when the input clock signal is determined to be a differential clock signal.

8. (original): The method of claim 5 wherein the generated clock signal has the same frequency as either as the first input clock signal or the second input clock signal.

9. (currently amended): A device comprising:

a first terminal to receive a first channel of a clock input signal;

a second terminal to receive a second channel of the clock input signal; and

a detector coupled to the second terminal to receive the second channel of the clock input signal, wherein the detector is configured to output a clock mode signal as a function of a

voltage potential of the second channel of the clock signal~~.~~, wherein the clock mode signal is coupled to a clock feedback matching circuit in a clock compensator.

10. (cancelled)

11. (amended): A device comprising:

a first terminal to receive a first clock input signal;

a second terminal to receive a second clock input signal;

a detector coupled to the second terminal to receive the second clock input signal, wherein the detector is configured to output a clock mode signal as a function of a voltage potential of the second clock signal;

a first circuit coupled to the first terminal configured to generate a first single-ended clock signal of the same frequency as the first clock input signal;

a second circuit coupled to the first terminal and to the second terminal to generate a second single-ended clock signal of the same frequency as the first clock input signal;

a selector configured to select the first single-ended clock signal or the second single-ended clock signal based upon the clock mode signal; and

~~The device of claim 10 further comprising~~ a clock generator coupled at least to the first terminal, configured to output a master clock signal.

12. (original): The device of claim 11, further comprising a compensator configured to receive the signal from either the first circuit or the second circuit and to output a core clock signal aligned with the master clock signal.

13. (original): The device of claim 12 wherein the compensator includes a phase-locked loop.

14. (original): The device of claim 12 wherein the compensator includes delay cancellation as a function of the clock mode signal.

15. (currently amended): The device of claim ~~10~~ 14 wherein the selector is a multiplexer.

16 - 19 (Cancelled)

20. (currently amended): A method comprising:

receiving an input clock signal representing either a differential clock signal or a single-ended clock signal;

determining whether the input clock signal is a differential clock signal or a single-ended clock signal; ~~and~~

automatically generating a clock mode signal based on the determination.~~;~~ and

aligning the input clock signal with an output clock signal.

21. (original): The method of claim 20 further comprising:

providing a first circuit for a single-ended clock signal, the output of the first circuit being a first output clock signal;

providing a second circuit for a differential clock signal, the output of the second circuit being a second output clock signal;

selecting either the output of the first circuit or the output of the second circuit as a function of the clock mode signal.

22. (currently amended): A method comprising:

receiving a first periodic clock signal voltage at a first input;

receiving at a second input one of a second periodic clock signal voltage, a constant signal voltage above ground potential or a constant ground potential signal;

detecting whether the signal received at the second input is a constant ground potential signal; ~~and~~

generating a clock mode signal indicative of the detection~~.~~; and

coupling the clock mode signal to a clock feedback matching circuit in a clock compensator.

23. (original): The method of claim 22 further comprising generating a high voltage clock mode signal when the signal received at the second input is a constant ground potential signal.

24 - 26 (Cancelled)

27. (previously presented): A system comprising:

a clock generator, wherein the clock generator issues one of a single-ended clock signal or a differential clock signal; and

an electronic device including a first input terminal and a second input terminal, with the first input terminal coupled to

the clock generator, the electronic device to generate a single-ended clock signal of the same frequency as the clock signal issued by the clock generator and aligned with the clock signal issued by the clock generator, wherein the electronic device includes a phase lock loop to compensate for delays in processing the clock generator clock signal so that the electronic device single-ended clock signal is aligned with the clock generator clock signal.

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28. (previously presented): A system comprising:

a clock generator, wherein the clock generator issues one of a single-ended clock signal or a differential clock signal; and

an electronic device including a first input terminal and a second input terminal, with the first input terminal coupled to the clock generator, the electronic device to generate a single-ended clock signal of the same frequency as the clock signal issued by the clock generator and aligned with the clock signal issued by the clock generator, wherein the electronic device couples the first input terminal to circuit ground when the clock generator issues a single-ended clock signal.

29. (previously presented): A system comprising:

a clock generator, wherein the clock generator issues one of a single-ended clock signal or a differential clock signal; and

an electronic device including a first input terminal and a second input terminal, with the first input terminal coupled to the clock generator, the electronic device to generate a single-ended clock signal of the same frequency as the clock signal

issued by the clock generator and aligned with the clock signal issued by the clock generator, wherein the electronic device first and second input terminals are coupled to the clock generator when the clock generator issues a differential clock signal.

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30. (previously presented): A method comprising:

receiving a clock signal, wherein the clock signal is one of a single-ended clock signal or a differential clock signal;

processing the clock signal wherein the processed clock signal has a time delay;

generating an output single-ended clock signal that follows the received clock signal; and

aligning the output single-ended clock signal with the received clock signal, wherein aligning includes compensating for the processed clock signal time delay, and wherein compensating includes providing adjustable feedback as a function of whether the received clock signal is the single-ended clock signal or the differential clock signal.